performed in a predetermined period after activating the reset signal, and length of the predetermined period being controlled by a first adjusting signal;

a voltage generator configured to receive an external power supply voltage for generating an internal supply voltage, the level of the internal supply voltage being controlled by a second adjusting signal;

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a programming circuit configured to output said first adjusting signal and said second adjusting signal; and

a signal selection circuit configured to receive an external signal, and to receive an external signal, and to receive said second adjusting signal from said programming circuit, to output the external signal to said voltage generator as said second adjusting signal in response to a test mode signal.

8. (Amended) The semiconductor integrated circuit according to claim 7, wherein said signal selection circuit includes a mask circuit for masking an output from said programming circuit and for outputting said external signal as said second adjusting signal, in response to said test mode signal which is activated during a testing mode.

A marked-up version of the claims is enclosed as required by 37 C.F.R. § 1.121.

REMARKS

Claims 1-9 are pending. By this Amendment claims 1, 7 and 8 have merely been amended to more particularly point out and distinctly claim the invention. No new matter is presented. Accordingly, claims 1-9 are presented for consideration.